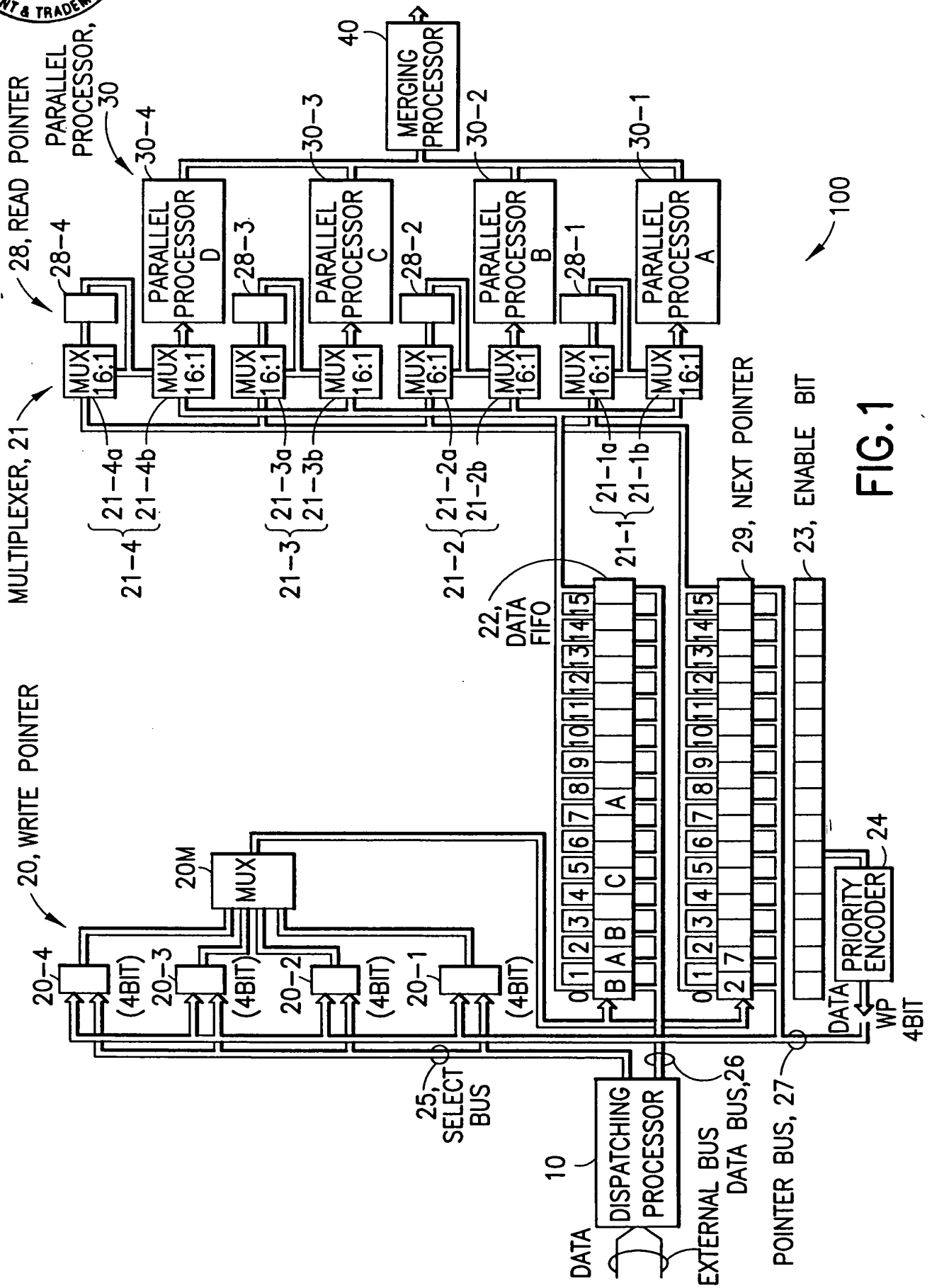


FIG. 1

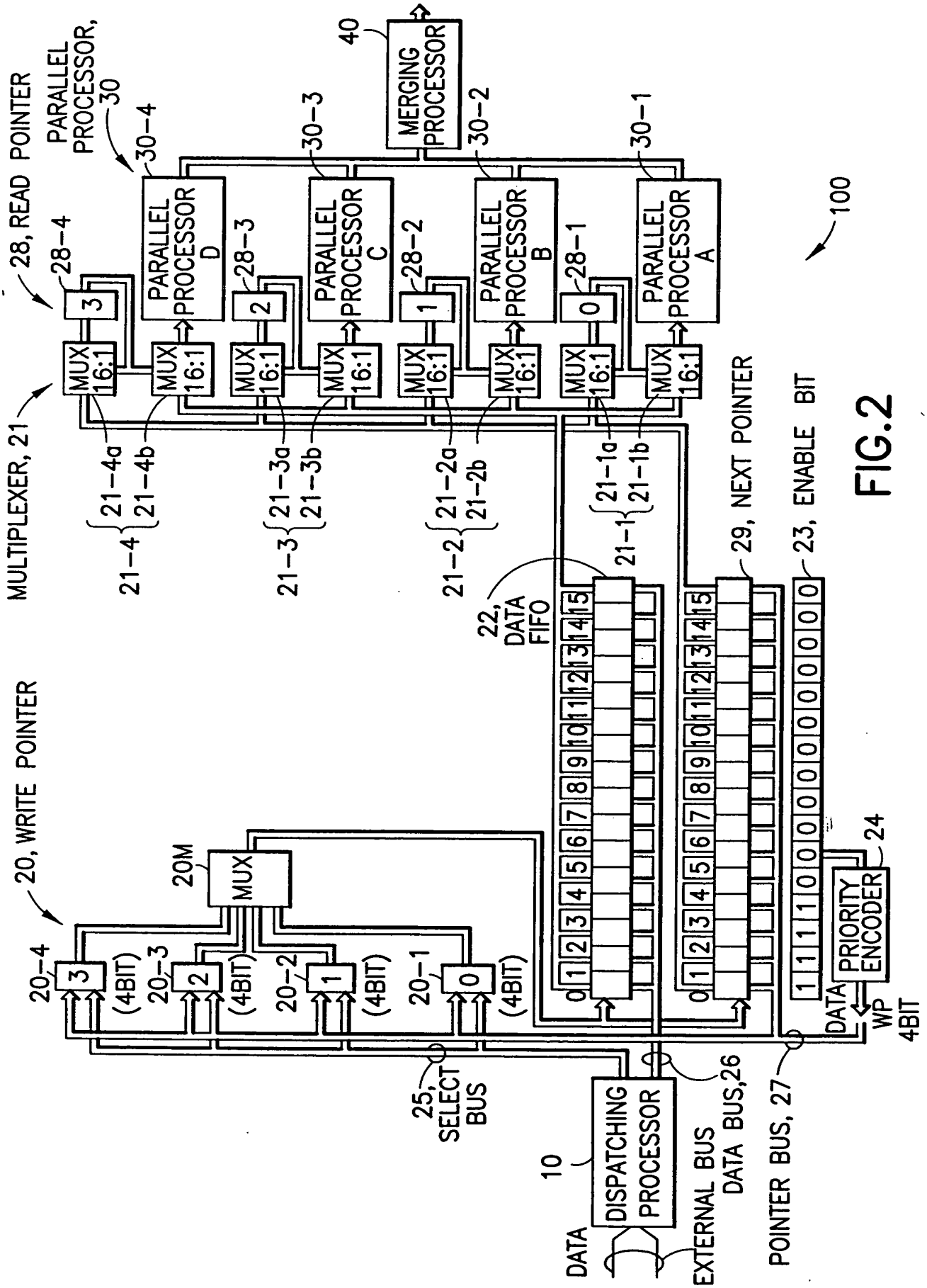
MULTIPLEXER, 21
28, READ POINTER
20, WRITE POINTER
PARALLEL PROCESSOR, 30
MERGING PROCESSOR
40
PARALLEL PROCESSOR A
PARALLEL PROCESSOR B
PARALLEL PROCESSOR C
PARALLEL PROCESSOR D
30-1
30-2
30-3
30-4
28-1
28-2
28-3
28-4
MUX 16:1
21-1a
21-1b
21-2a
21-2b
21-3a
21-3b
21-4a
21-4b
22, DATA FIFO
29, NEXT POINTER
23, ENABLE BIT
PRIORITY ENCODER
24
DATA
WP
4BIT
20M
MUX
20-1
20-2
20-3
20-4
(4BIT)
25, SELECT BUS
10
DISPATCHING PROCESSOR
DATA
EXTERNAL BUS DATA BUS, 26
POINTER BUS, 27
100

FIG.2

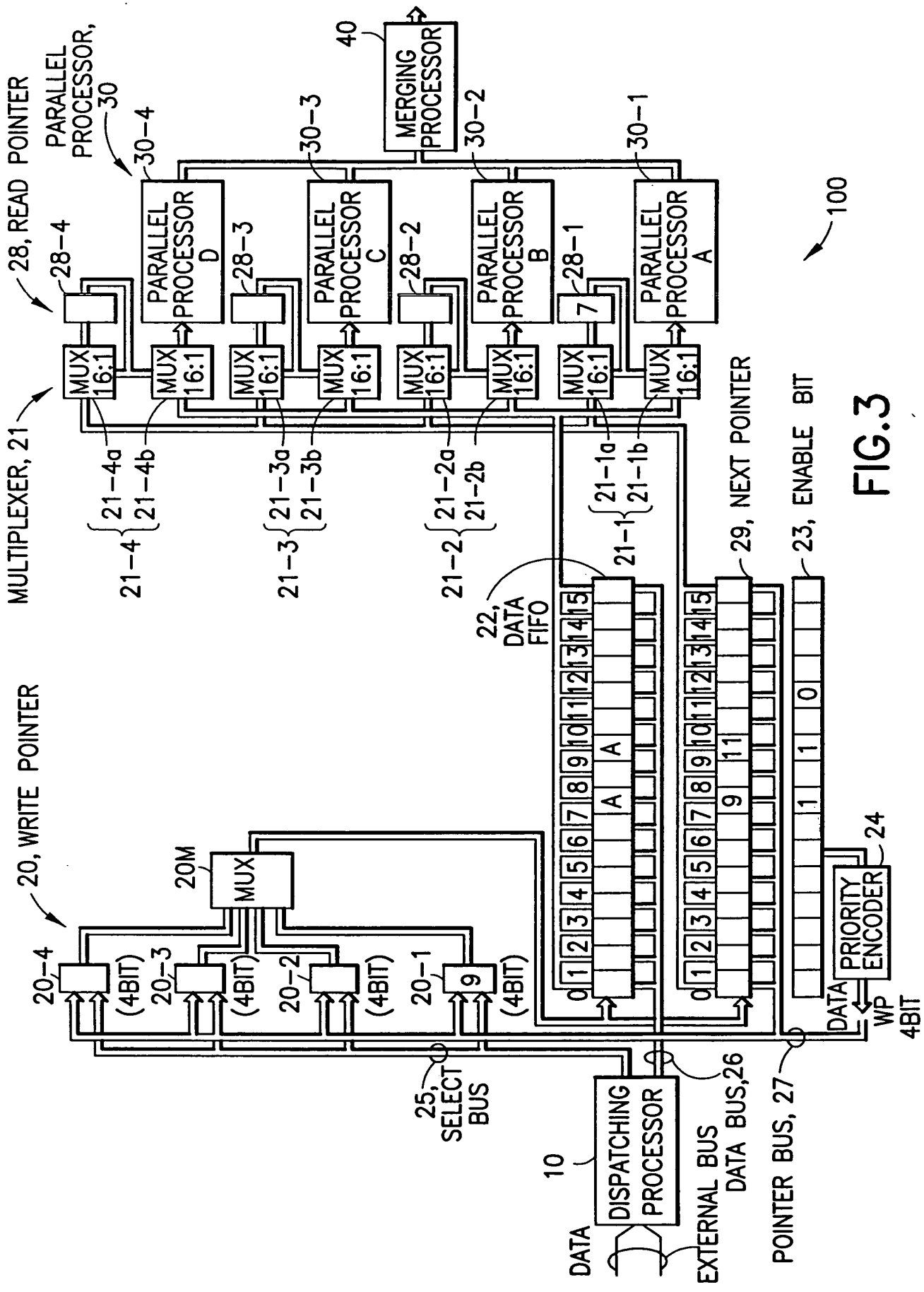
28, READ POINTER
PARALLEL PROCESSOR, 30
30-4
30-3
30-2
30-1
40
MERGING PROCESSOR
28-4
28-3
28-2
28-1
PARALLEL PROCESSOR D
PARALLEL PROCESSOR C
PARALLEL PROCESSOR B
PARALLEL PROCESSOR A
100
MUX 16:1
MULTIPLEXER, 21
21-4a
21-4b
21-4
21-3a
21-3b
21-3
21-2a
21-2b
21-2
21-1a
21-1b
21-1
22, DATA FIFO
29, NEXT POINTER
23, ENABLE BIT
20, WRITE POINTER
20M
MUX
20-4
20-3
20-2
20-1
(4BIT)
PRIORITY ENCODER
24
DATA
WP
4BIT
25, SELECT BUS
10
DISPATCHING PROCESSOR
DATA
EXTERNAL BUS
DATA BUS, 26
POINTER BUS, 27

FIG.3

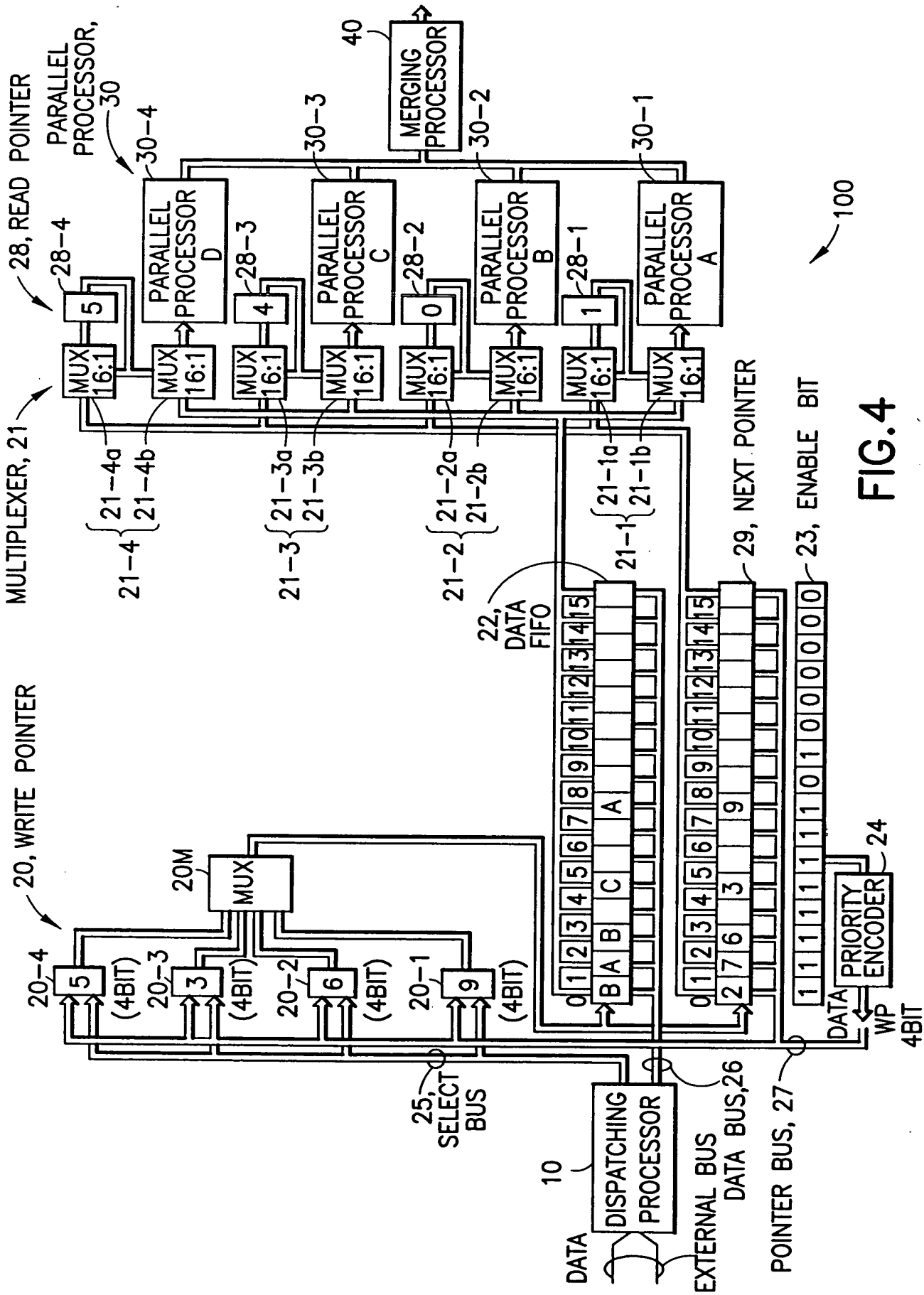
MERGING PROCESSOR
40
PARALLEL PROCESSOR, 30
30-4
30-3
30-2
30-1
PARALLEL PROCESSOR D
PARALLEL PROCESSOR C
PARALLEL PROCESSOR B
PARALLEL PROCESSOR A
28, READ POINTER
28-4
28-3
28-2
28-1
MUX 16:1
MULTIPLEXER, 21
21-4a
21-4b
21-4
21-3a
21-3b
21-3
21-2a
21-2b
21-2
21-1a
21-1b
21-1
22, DATA FIFO
29, NEXT POINTER
23, ENABLE BIT
100
20, WRITE POINTER
20M
MUX
20-4
20-3
20-2
20-1
(4BIT)
PRIORITY ENCODER
24
DATA
WP
4BIT
25, SELECT BUS
10
DISPATCHING PROCESSOR
DATA
EXTERNAL BUS DATA BUS, 26
POINTER BUS, 27

FIG. 4

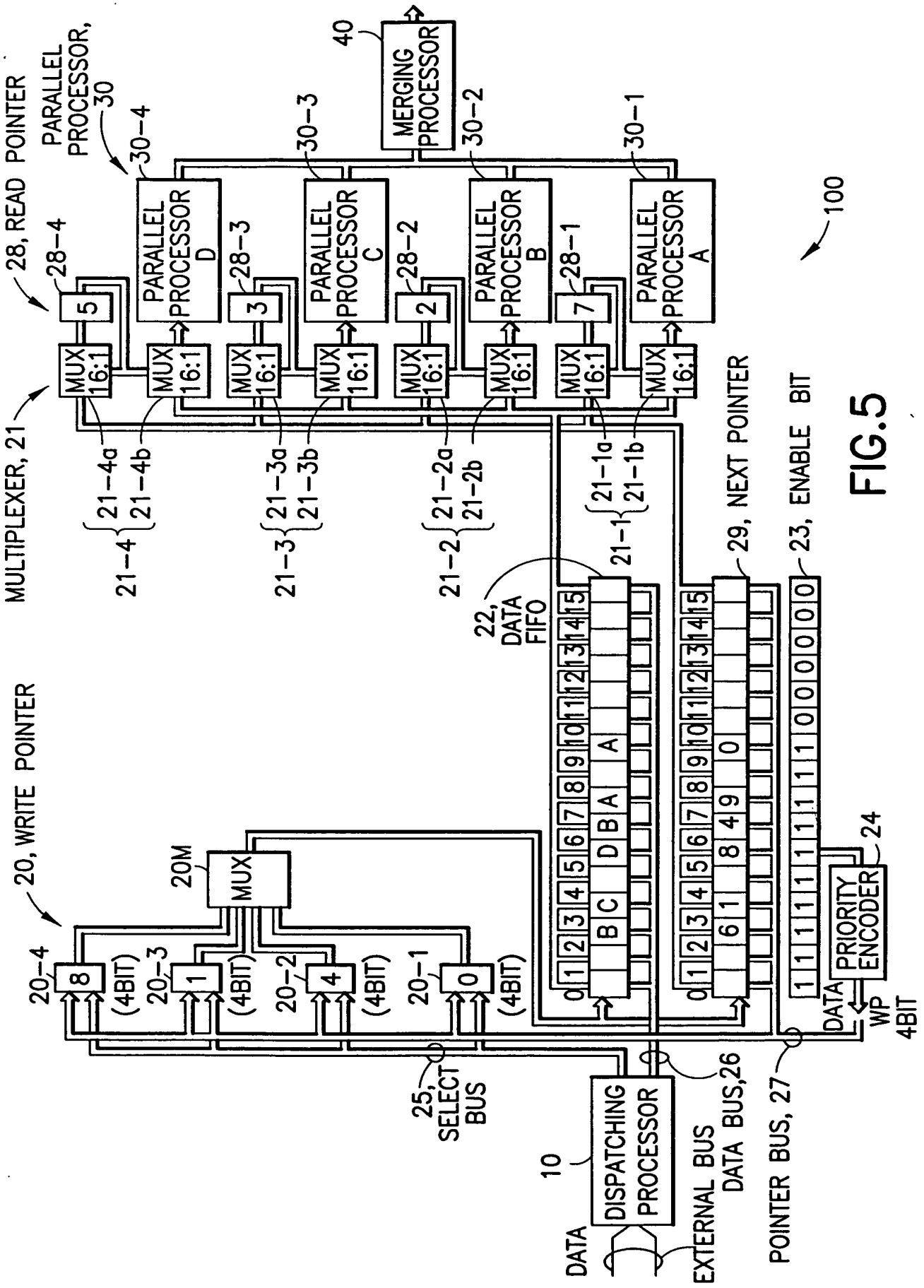
100
MULTIPLEXER, 21
28, READ POINTER
PARALLEL PROCESSOR, 30
MERGING PROCESSOR
40
30-4
30-3
30-2
30-1
PARALLEL PROCESSOR D
PARALLEL PROCESSOR C
PARALLEL PROCESSOR B
PARALLEL PROCESSOR A
28-4
28-3
28-2
28-1
MUX 16:1
21-4a
21-4b
21-4
21-3a
21-3b
21-3
21-2a
21-2b
21-2
21-1a
21-1b
21-1
22, DATA FIFO
29, NEXT POINTER
23, ENABLE BIT
20, WRITE POINTER
20M MUX
20-4
20-3
20-2
20-1
(4BIT)
PRIORITY ENCODER
24
DATA
WP
4BIT
25, SELECT BUS
10
DISPATCHING PROCESSOR
DATA
EXTERNAL BUS
DATA BUS, 26
POINTER BUS, 27

FIG.5

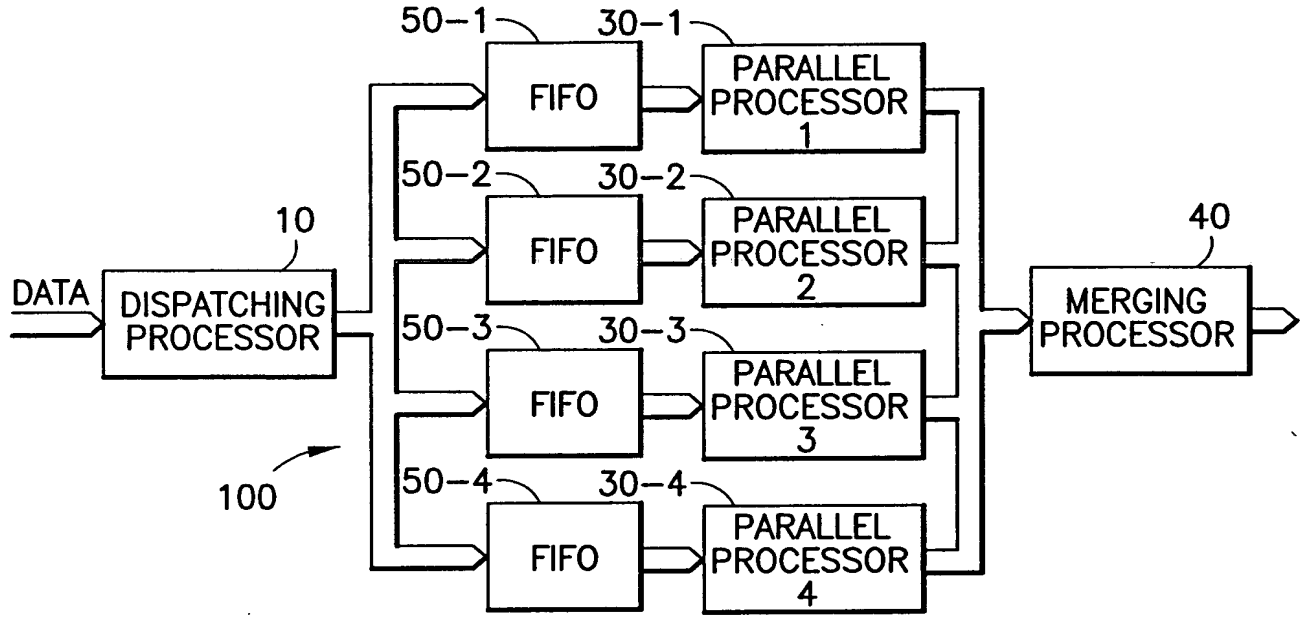


FIG.6

| | CASE(a) | CASE(b) | CASE(c) |
|---|---|---|---|
| PARALLEL PROCESSOR 1 | 1 | 2 | 2 |
| PARALLEL PROCESSOR 2 | 3 | 1 | 8 |
| PARALLEL PROCESSOR 3 | 2 | 5 | 1 |
| PARALLEL PROCESSOR 4 | 1 | 1 | 3 |

FIG.7

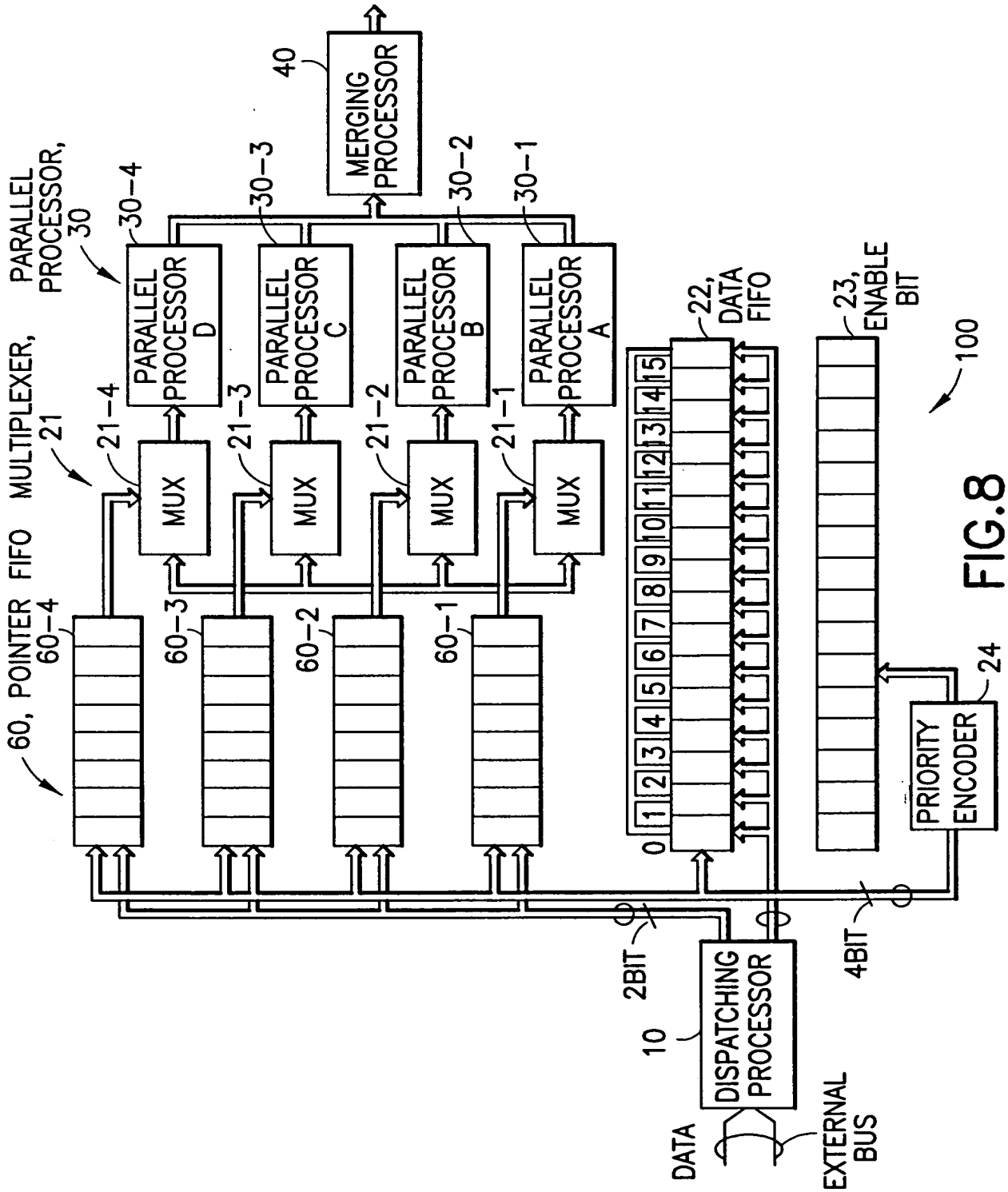
40
MERGING PROCESSOR
PARALLEL PROCESSOR, 30
30-4
30-3
30-2
30-1
PARALLEL PROCESSOR D
PARALLEL PROCESSOR C
PARALLEL PROCESSOR B
PARALLEL PROCESSOR A
MULTIPLEXER, 21
21-4
21-3
21-2
21-1
MUX
60, POINTER FIFO
60-4
60-3
60-2
60-1
22, DATA FIFO
23, ENABLE BIT
100
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
PRIORITY ENCODER
24
2BIT
4BIT
10
DISPATCHING PROCESSOR
DATA
EXTERNAL BUS

FIG.8